Validated 90nm CMOS Technology Platform with Low-k Copper Interconnects for Advanced System-on-Chip (SoC)

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Abstract

This paper presents a complete 90nm CMOS technology platform dedicated to advanced SoC manufacturing, featuring 16Å EOT-70nm transistors (standard process) or 21Å-90nm transistors (Low Power process) as well as 2.5 or 3.3V I/O transistors, copper interconnects and SiOC low-k IMD (k=2.9). The main critical process steps are described and electrical results are discussed. Moreover, using advanced lithographic tools, fully functional 1Mbit SRAM instances, based on a highly manufacturable 6T 1.36µm² memory cell, have been processed. The cell is detailed and its features, both electrical and morphological, are discussed.

Process integration

The strong demand for total solution SoC results in a continuously increased technology complexity. The concerns are both system performance and stand-by power, as well as convenient chip interfaces. This requires different transistor flavors, low-k IMD, multi power supply management, triple well technology, as well as powerful embedded memories. The technology platform presented in this work is a 90nm CMOS process suitable for both logic and analog applications that support 2.5V or 3.3V I/O circuits. In fact, the offer is twofold : a General Purpose platform featuring a 16Å EOT gate oxide with 70nm gate length 1.0V transistors suitable for ASIC applications and a Low Power one featuring 21Å - 90nm 1.2V transistors suitable for mobile applications. For both platforms, two transistor flavors are proposed, allowing stand-by power management : a high speed and a low leakage transistor, using multiple Vt adjustments (see Table I).

Table I : 90nm CMOS platform

	General Purpose		Low Power	
	Low Vt	Nom Vt	Low Vt	Nom Vt
Vdd (V)	1.0		1.2	
Tox (A) optical	16		21	
Lgate (nm)	≤ 70		≤ 90	
NMOS				
Ion (µA/µm)	640	520	540	415
Ioff (nA/µm)	10	1	0.4	0.01
Jg (A/cm²)	2		0.005	
PMOS				
Ion (µA/µm)	280	215	250	170
Ioff (nA/µm)	10	1	0.4	0.01
Jg (A/cm²)	1		0.002	

Table II : Main design Rules

	Design Rule		SRAM	
	Line	Space	Line	Space
Active	0.12	0.14	0.12	0.14
Poly	0.10	0.14	0.11	0.27*
Contact	0.12	0.14	0.12	0.14
M1	0.12	0.12	0.16	0.14
Via1-Via6	0.13	0.15	0.13	0.30
M2-M7	0.14	0.14	0.18	0.18
Via7-Via8	0.36	0.34		
M8-M9	0.42	0.42		
PO Endcap	0.16	0.14	0.14	0.12
Poly-CT		0.08		0.075
N+/P+		0.44		0.30

* Except Poly Endcap Space

The process flow is based on a standard CMOS process with STI, retrograde Arsenic and Boron/Indium channels and a modular dual gate oxide process. 70nm or 90nm gate lengths are obtained from a resist trimming performed on 0.1µm printed lines (see Fig. 1). After gate patterning, ULE Ldd implants with As and BF_2, coupled with heavy ion pockets to control Short Channel Effect (SCE) are performed. Nitride L-shape spacers are formed

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before S/D Implant. Activation is performed through a high temperature spike anneal to control P-type S/D extensions, while maintaining a high level of dopant activation. $CoSi_2$ is then formed. Finally W plugs contact a single damascene copper Metal1 (see Fig. 2).

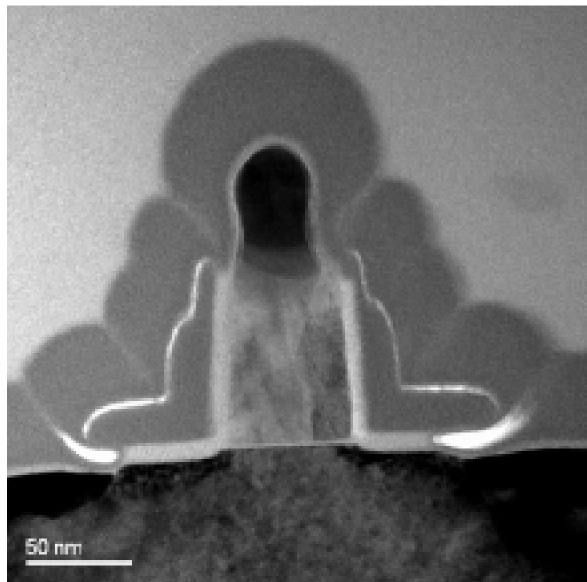

Fig. 1 : TEM cross-section of a 70nm transistor

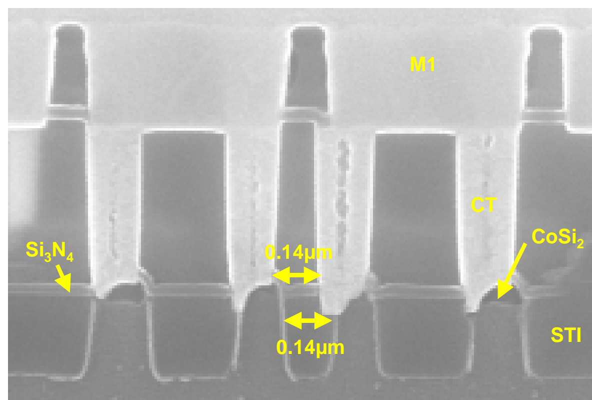

Fig. 2 : SEM cross-section in SRAM, showing minimum space for Active and Contact

Devices Performances

The 16Å EOT gate oxide is formed through an NO Rapid Thermal Nitridation of a thermal pre-oxide, resulting in a well controlled gate leakage (<2A/cm²@1V) and breakdown voltage higher than 12MV/cm (see Fig. 3).

The introduction of such a thin oxide allows a better control of the Short Channel Effects. Fig. 5 illustrates this in the Vt-L plots obtained for gates drawn down to 0.1µm. The Ion-Ioff plots in Fig. 4 correspond to high Vt transistors used in the SRAM periphery. Ion of 535 and 225µA/µm are obtained for NMOS and PMOS respectively for a maximum leakage of 10nA/µm.

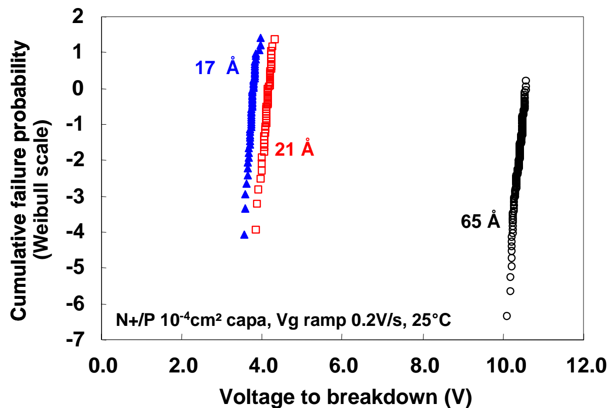

Fig. 3 : Oxides integrity figures for the different oxides

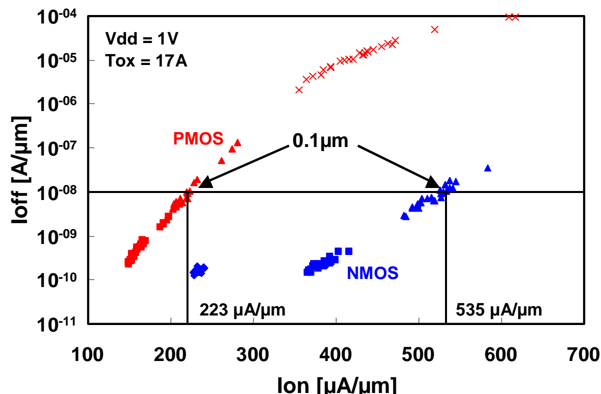

Fig. 4 : SRAM transistors Ion-Ioff figures for the General Purpose process

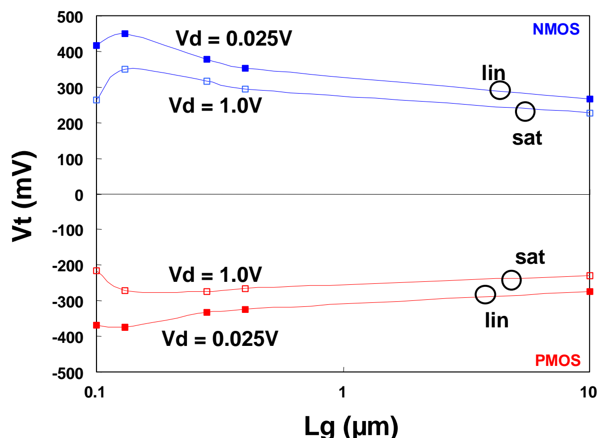

Fig. 5 : Vt-L figures for nominal Vt transistors from the General Purpose process

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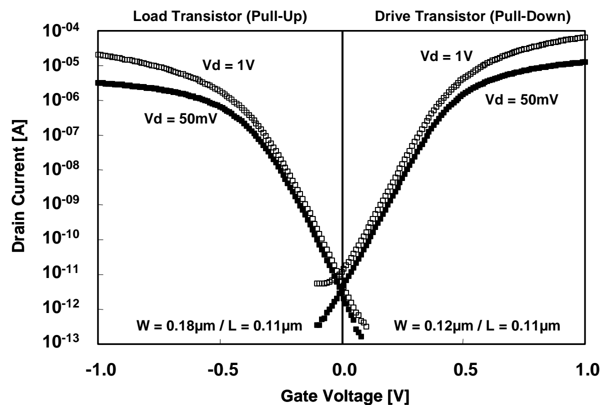

Fig. 6 : SRAM transistors transfer characteristics

For the SRAM cell transistors, the leakage is further reduced by using a specific Vt implant (See Fig. 6).

It can be noticed that SRAM devices exhibit a good sub-threshold behavior, in particular with a very low Drain Induced Barrier Lowering (DIBL) for both NMOS and PMOS.

Copper / SiOC low-k interconnects

Fig. 7 presents a SEM cross-section of fully integrated low k SiOC dielectric (k~2.9) carried out on 3 levels of copper. Dual Damascene (DD) Via First architecture is used, including an I-line resist Via refill process to protect the bottom of Vias during trench etching. A thin etch-stop layer of SiC is deposited in an integrated equipment along with SiOC. SiC is preferred to SiCN for 3 main reasons: it has a lower dielectric constant, higher etch selectivity with respect to SiOC, and thanks to a lower [H] content, its compressive stress component is better matched to SiOC facilitating packaging issues. Via poisoning was suppressed through proper choice of resist processing and well-suited etching [1]. The DD architecture cleaning was followed by advanced PVD of a TaN/Ta bi-layer diffusion barrier and a continuous PVD copper seed layer. Copper filling was achieved through controlled electroplating and recrystallisation annealing ensuring void-free low-resistance filling. CMP processing and post cleanings remove excess copper and stabilize the exposed metal. Fig. 9 shows a Via resistance boxplot corresponding to 0.18µm diameter Via2 chains. Via resistance is 2-3Ω with little spread. Fig. 8 confirms the absence of line-to-line leakage. Finally measured line-to-line capacitance show a 25% reduction when going from our standard industrial FSG/SiN/copper process to the SiOC/SiC integration.

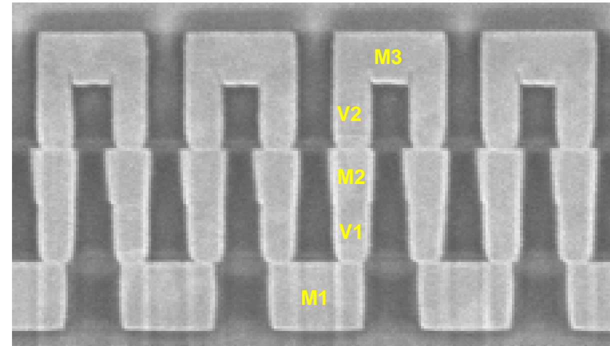

Fig. 7 : Cu / SiOC interconnects cross-section

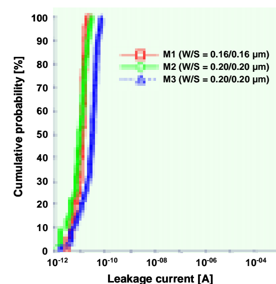

Fig. 8 : Metal-Metal leakage

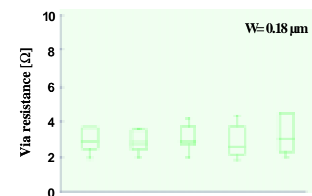

Fig. 9 : Via resistance

High Density Memory Cells Integration

The memory cell is a key feature of the technology platform. Its size, of course, is of crucial importance, since the SRAM is becoming a predominant area contributor in most of the products. However, some other features are to be taken into account like its manufacturability. Indeed, the way the cell is designed has a major impact on the different process windows related to its manufacturing, and therefore to the related yield, especially in case of high density designs, i.e. using SRAM cell dedicated design rules. Moreover, it also determines major cell electrical parameters like the Static Noise Margin (SNM), though the devices matching performance, as well as the spread of any other electrical parameters.

In this regard, a comparison study has been performed in [2] between a few among the most common cells. The so-called type-1 cell, which is probably the most common one (see Fig. 10), is subject to Active rounding and is therefore highly sensitive to misalignment, resulting in enhanced mismatch. Moreover, a quite aggressive metal 1 pitch is required.

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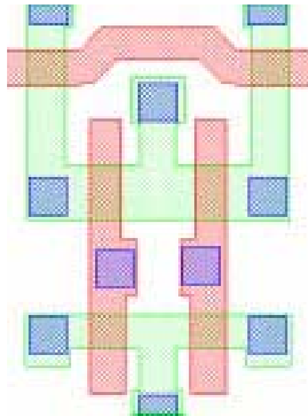
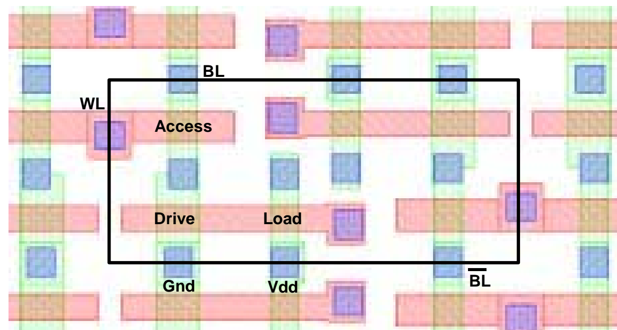


Fig. 10 : Type-1 cell basic layout with Active, Poly and Contact

This is why a type-4 cell has been preferred for a while (see Fig. 11). Indeed, it allows very careful devices control (straight poly lines crossing straight active lines) as well as relaxed Back-End pitches (see Table II), i.e. it is highly manufacturable.

Moreover, the shrink of such a cell is quite straightforward and we believe that aggressive cell dimensions can be more easily obtained.



(a) Poly, Active and Contact

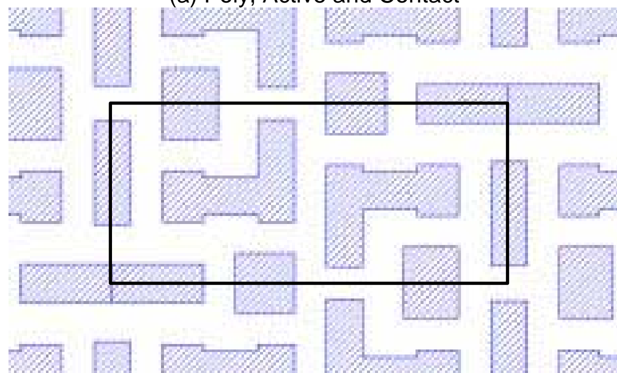

(b) Metal 1

Fig. 11 : 1.36µm² MemCell basic layout (Type-4 cell)

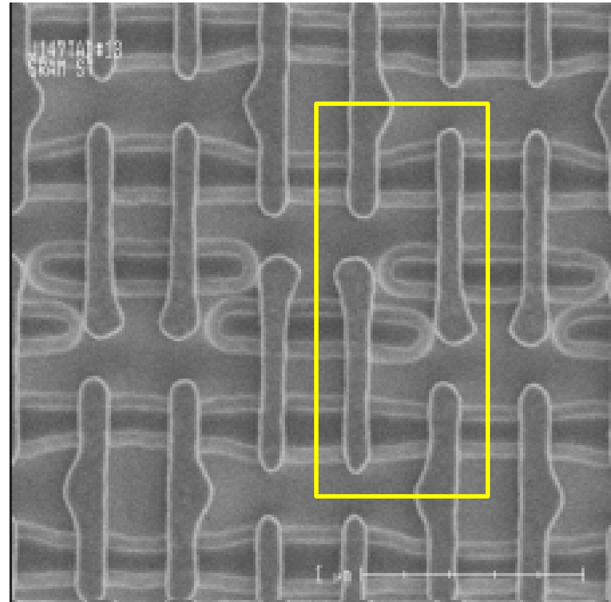
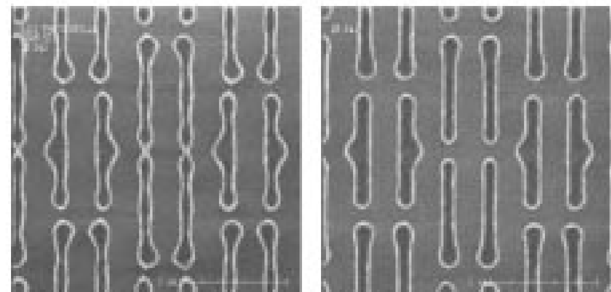


Fig. 12 : 1.36µm² MemCell SEM Top View, after Poly patterning


(a) Gate Photo. Left : First guess OPC – Right : First iteration OPC

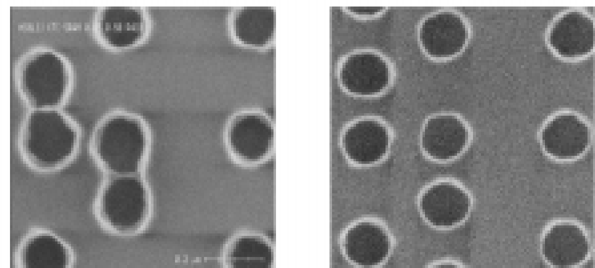

(b) Contact photo. Left : w/o PSM – Right : with PSM

Fig. 13 : (a) OPC and (b) attenuated PSM improvements

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Fig. 11 shows a SEM picture of such a cell with its straight Poly and Active lines. In fact, even if a 193nm lithography solution has been developed for all the critical levels (Active, Poly, Contact and Metals), more advanced techniques have been required as long as targeted dimensions go below the wavelength of exposure. A model based OPC strategy has been employed for these levels. As the SRAM cell is often the most critical structure in a design, a good interaction between the design of the memcell and the OPC model approach is necessary, as shown in Fig. 12a. In the same way, the use of attenuated Phase Shift Mask (PSM) can improve the lithographic resolution for a few levels like Contact (see Fig. 12b).

Fig. 14 shows statistical data from the three devices from the memory cell. It is interesting to note that these well controlled device dimensions result in low electrical parameters spread. It is also a key factor in the good sub-threshold behavior depicted in Fig. 6.

Besides, butterfly characteristics of this memory cell are presented in Fig. 15 for supply voltages ranging from 0.7V to 1.4V and the statistical distribution of the Static Noise Margin extracted from these curves are also shown in Fig. 16. Here again, a low spread is obtained, while the SNM central values are well above any mass production requirement criteria.

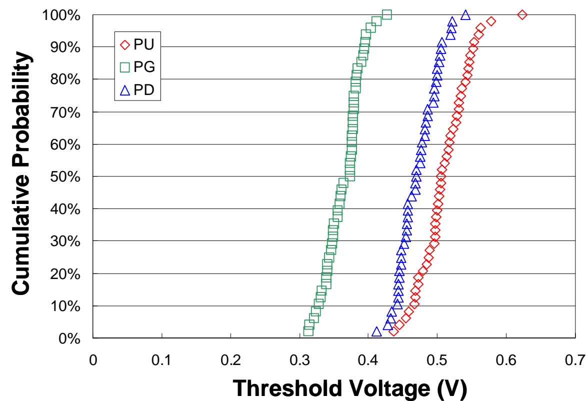

Fig. 14 : Threshold voltage cumulative plot from the three SRAM devices

Finally, a 1Mbit SRAM instance based on this memory cell have been already successfully manufactured. Fig. 16 is presenting a shmoo plot of such an instance showing complete functionality in a wide range of supply voltage.

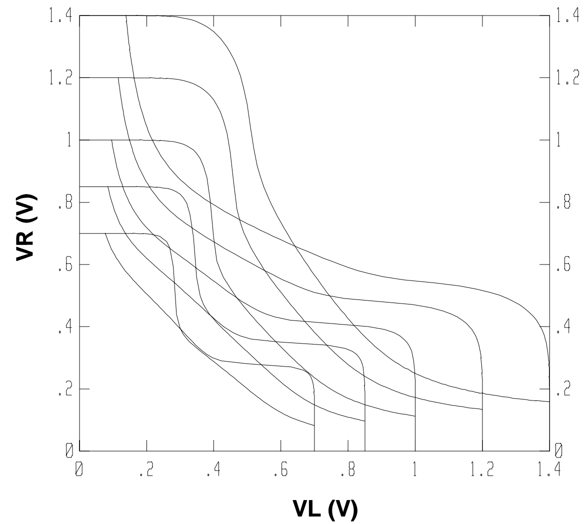

Fig. 15 : 1.36µm² MemCell measured Butterfly characteristics for supply voltages ranging from 0.7 to 1.4V

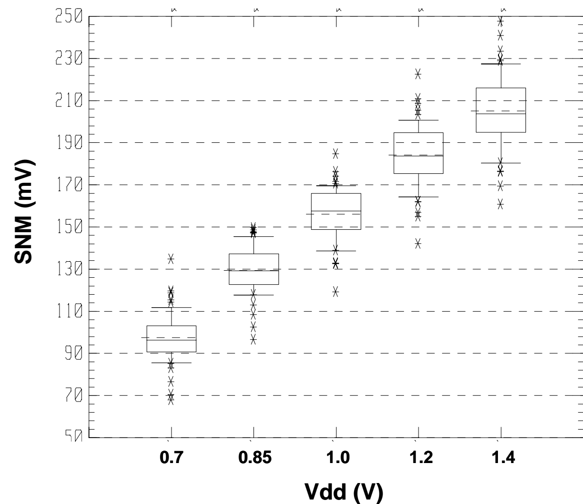

Fig. 16 : SNM distribution as a function of the supply voltage

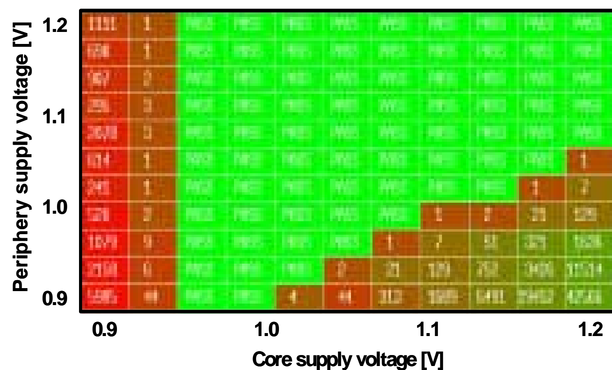

Fig. 17 : SRAM cut shmoo plot showing functionality in a wide range of supply voltage

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Conclusion

A complete 90nm CMOS technology platform dedicated to advanced SoC manufacturing has been presented featuring copper interconnects and SiOC low-k IMD (k=2.9). 16Å EOT-70nm transistors for the General Purpose process or 21Å-90nm transistors for the Low Power process are proposed as well as 2.5 or 3.3V compatible I/O transistors. Besides, a highly manufacturable 1.36µm² SRAM memory cell has been presented. Its strengths in terms of devices control as well as relaxed Back-End pitches (for yield maximization) have been discussed and fully functional 1Mbit SRAM instance based on this cell have been demonstrated.

Acknowledgments

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